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571-203-2790

December 31, 2003

ATTORNEY DOCKET NO. 09407.0001
CUSTOMER NO. 22,852

Mail Stop Patent Application

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

17510 10/748241 US PTO
123103

New U.S. Patent Application
Title: METHOD FOR FABRICATING TRANSISTOR OF
SEMICONDUCTOR DEVICE

Inventor and Address:

Jeong Ho PARK
Gyeonggi-do, Korea

Sir:

We enclose the following papers for filing in the United States Patent and Trademark Office in connection with the above patent application.

1. Application- 26 pages, including 3 independent claims and 31 claims total.
2. Drawings- 8 sheets of drawings containing 22 figures
3. The filing fee is calculated as follows:

Basic Application Filing Fee					\$770	\$ 770.00
	Number of Claims		Basic	Extra Claims		
Total Claims	31	-	20	11	x \$18	198.00
Independent Claims	3	-	3		x \$86	
<input type="checkbox"/> Presentation of Multiple Dep. Claim(s)					+\$290	
Subtotal						\$ 968.00
Reduction by 1/2 if small entity						-
TOTAL APPLICATION FILING FEE						\$ 968.00

4. A check for \$968.00 is enclosed.

This application is being filed under the provisions of 37 C.F.R. § 1.53(f).
Applicant awaits notification from the Patent and Trademark Office of the time set for
filing the Declaration.

Applicant claims the right to priority based on Korean Patent Application No. 10-2003-0075431, filed October 28, 2003, Korean Patent Application No. 10-2003-0075440, filed October 28, 2003 and Korean Patent Application No. 10-2003-0078770, filed November 7, 2003.

Please address all correspondence with respect to this application to:

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Please accord this application an application number and filing date.

The Commissioner is hereby authorized to charge any additional filing fees due
and any other fees due under 37 C.F.R. § 1.16 or §1.17 during the pendency of this

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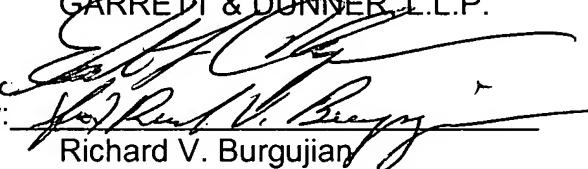
FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

application to our Deposit Account No. 06-0916.

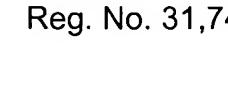
Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

By:


Richard V. Burgujian
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RVB/FPD/dvg
Enclosures


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